CLAIMS:

What is claimed is:

1. A method of swapping out a memory region in a system area network, comprising:

instructing a process to inhibit further operations to the memory region;

determining if a current number of outstanding operations to the memory region is zero; and

swapping out the memory region if the current number of outstanding operations to the memory region is zero.

2. The method of claim 1, wherein instructing the process to inhibit further operations to the memory region includes setting a quiesce indicator for the memory region.

3. The method of claim 2, wherein the quiesce indicator is located in a fixed memory in association with the memory region.

4. The method of claim 2, wherein the quiesce indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

5. The method of claim 4, wherein determining if a current number of outstanding operations to the memory region is zero includes determining if the current outstanding operation count is zero.

6. The method of claim 1, wherein swapping out the memory region includes setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

7. The method of claim 1, wherein swapping out the memory region includes deregistering the memory region.

8. The method of claim 1, further comprising:
swapping in the memory region;
updating an address translation table based on the swapping in of the memory region.

9. The method of claim 2, further comprising:
swapping in the memory region; and
resetting the quiesce indicator to allow further operations to the memory region.

10. The method of claim 6, further comprising:
swapping in the memory region; and
resetting the valid bit to indicate the memory region is valid.

11. A computer program product in a computer readable medium for swapping out a memory region in a system area network, comprising:
first instructions for instructing a process to inhibit further operations to the memory region;
second instructions for determining if a current number of outstanding operations to the memory region is zero; and

third instructions for swapping out the memory region if the current number of outstanding operations to the memory region is zero.

12. The computer program product of claim 11, wherein the first instructions for instructing the process to inhibit further operations to the memory region include instructions for setting a quiesce indicator for the memory region.

13. The computer program product of claim 12, wherein the quiesce indicator is located in a fixed memory in association with the memory region.

14. The computer program product of claim 12, wherein the quiesce indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

15. The computer program product of claim 14, wherein the second instructions for determining if a current number of outstanding operations to the memory region is zero include instructions for determining if the current outstanding operation count is zero.

16. The computer program product of claim 11, wherein the third instructions for swapping out the memory region include instructions for setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

17. The computer program product of claim 11, wherein the third instructions for swapping out the memory region include instructions for deregistering the memory region.

18. The computer program product of claim 11, further comprising:

fourth instructions for swapping in the memory region;

fifth instructions for updating an address translation table based on the swapping in of the memory region.

19. The computer program product of claim 12, further comprising:

fourth instructions for swapping in the memory region; and

fifth instructions for resetting the quiesce indicator to allow further operations to the memory region.

20. The computer program product of claim 16, further comprising:

fourth instrucions for swapping in the memory region; and

fifth instructions for resetting the valid bit to indicate the memory region is valid.

21. An apparatus for swapping out a memory region in a system area network, comprising:

means for instructing a process to inhibit further operations to the memory region;

means for determining if a current number of outstanding operations to the memory region is zero; and

means for swapping out the memory region if the current number of outstanding operations to the memory region is zero.

22. The apparatus of claim 21, wherein the means for instructing the process to inhibit further operations to the memory region includes means for setting a quiesce indicator for the memory region.

23. The apparatus of claim 22, wherein the quiesce indicator is located in a fixed memory in association with the memory region.

24. The apparatus of claim 22, wherein the quiesce indicator is located in fixed memory in association with a current outstanding operation count for the memory region.

25. The apparatus of claim 24, wherein the means for determining if a current number of outstanding operations to the memory region is zero includes means for determining if the current outstanding operation count is zero.

26. The apparatus of claim 21, wherein the means for swapping out the memory region includes means for setting a valid bit in a protection table entry associated with the memory region to indicate the memory region is invalid.

27. The apparatus of claim 21, wherein the means for swapping out the memory region includes means for deregistering the memory region.

28. The apparatus of claim 21, further comprising:

means for swapping in the memory region;

means for updating an address translation table based on the swapping in of the memory region.

29. The apparatus of claim 22, further comprising:

means for swapping in the memory region; and

means for resetting the quiesce indicator to allow further operations to the memory region.

30. The apparatus of claim 26, further comprising:

means for swapping in the memory region; and

means for resetting the valid bit to indicate the memory region is valid.